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09/801,241	03/07/2001	David Latta	ARC.003A	5003

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EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,241	LATTA, DAVID	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,25 and 31-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,25 and 31-46* is/are rejected.

7)☒ Claim(s) *37-40 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment to the claims filed on May 26, 2004 does not comply with the requirements of 37 CFR 1.121(c) because the identifier "previously presented" is used where "original" should have been used. The identifier "previously presented" should be used for claims that were previously added or amended in an earlier amendment paper, whereas "original" should be used for claims filed with the original specification. Amendments to the claims filed on or after July 30, 2003 must comply with 37 CFR 1.121(c).

Specification

2. The disclosure is objected to because of the following informalities:

Each of the terms of the acronym "HDL" (*e.g.*, on page 5, line 27) should be spelled out at the first occurrence of the acronym in the specification.

Appropriate correction is required. See 37 CFR 1.71.

Claim Objections

3. Claims 37-40 and 46 objected to because of the following informalities:

Claim 37 recites "DSP" in line 2. Each of the terms of the acronym "DSP" should be spelled out at the first occurrence of the acronym in the claims.

Claim 38 recites "an software wrapper" in line 1. Change "an" to --a--.

Claim 39 recites "HDL" in line 2 (two occurrences). Each of the terms of the acronym "HDL" should be spelled out at the first occurrence of the acronym in the claims.

Claim 40 recites "RISC" in line 3. Each of the terms of the acronym "RISC" should be spelled out at the first occurrence of the acronym in the claims.

Claim 46 recites "RISC" in line 2. Each of the terms of the acronym "RISC" should be spelled out at the first occurrence of the acronym in the claims.

Appropriate correction is required. See 37 CFR 1.75.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 31-36 and 38-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 31 recites the limitation "said configuration" in line 13. There is insufficient antecedent basis for this limitation in the claim.

7. Claims 32-36 inherit the deficiencies of claim 31.

8. Claim 38 recites the limitation "said DSP" in line 2. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 39 inherits the deficiencies of claim 38.

10. Claim 40 recites the limitation "said user-configuration" in lines 13-14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,628,662 to Blackmon, et al. ("Blackmon").

With regard to claim 18, Blackmon discloses a method of accessing data disposed within X and Y memory banks as respective first and second pages (Fig. 1, items 16a-16n), including; providing at least first and second macro functions adapted to process data (Fig. 1, item 10a-10b); providing a memory interface having at least two function ports and two memory ports (Fig. 2, items A-F), each of said memory ports being in data communication with respective ones of said memory banks, each of said function ports being capable of data communication with each of said memory ports, said first and second macro functions being in data communication with respective ones of said at least two function ports (see generally, Fig. 2); controlling the operation of said first and second macro functions using at least one parent processor instruction; and

simultaneously accessing said pages of data disposed within respective ones of said memory banks using respective ones of said macro functions such that two operand sources are provided simultaneously (column 3, lines 31-44). (*See generally*, the text accompanying Figs. 1 and 2).

With regard to claim 19, Blackmon discloses the method, further including arbitrating access to said at least two memory ports by said at least first and second function ports using a crossbar (Fig. 1, item 14 and Fig. 2, items 32, 34, and 36).

Therefore, Blackmon reads on the invention as claimed.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-4, 9, 10, 14, 15, 20-22, 25, 31-34, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of U.S. Patent No. 5,848,289 to Studor, et al. ("Studor").

With regard to claims 1, 9, 10, 25, 31, and 44, Blackmon discloses a processor interface device (Fig. 1, item 8) and a method of accessing data disposed within a plurality of memory banks. The processor interface device includes at least one memory port (Fig. 2, items E and F), the memory ports adapted to transfer data and signals to and from a storage device (Fig. 1, items 16a-16n), at least one function port

(Fig. 2, items A, B, C, and D), the function ports adapted to transfer data and signals to and from a macro function (Fig. 1, items 10a-10d), a data transfer fabric (Fig. 1, item 14 and Fig. 2, item 30) adapted to transfer data and signals between the memory ports and the function ports, and an arbitration unit (Fig. 2, items 32, 34, and 36) adapted to arbitrate access to various portions of the storage device by the macro functions.

With regard to claims 2-4, 14, 15, 32-34, and 45, Blackmon discloses a processor interface device, where the data transfer fabric is a crossbar switch fabric (Fig. 1, item 14), and where the processor interface device further includes a macro function in data communication with the function ports (column 3, lines 48-50), the macro function being controlled at least in part by a processor instruction associated with the macro function, where the macro function may access the at least one memory port. The processor interface device also further includes a plurality of macro functions (column 3, lines 48-50) in data communication with respective ones of the function ports, the interface device further adapted to allow simultaneous access to multiple ones of the memory ports (column 3, lines 56-67 to column 4, lines 1-3) by respective ones of the macro functions via the function ports.

Blackmon does not expressly disclose where the processor interface device is used in an extensible processor.

Studor discloses an extensible processor (*see generally*, Fig. 2).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the extensible processor of Studor with the processor interface device of Blackmon. The suggestion or motivation for doing so would have been to

allow a prior art CPU to be made extensible so that circuitry can be easily added to the extensible processor in order to meet differing customer needs, both in the present and in the future. This significantly reduces the cost for individual customer flexibility (*see* column 2, lines 57-67 and column 3, lines 38-43).

As described above with regard to the anticipation rejection, Blackmon discloses all the features of claim 18.

With regard to claims 20-22, Blackmon does not expressly disclose where the act of controlling includes initiating at least one of said first and second macro functions using an instruction decoded in the instruction decode stage of the parent processor; where the act of controlling further includes controlling at least one of said macro functions based at least in part on one immediate operand derived from the decoded instruction; or where the act of controlling includes accessing at least one extension register resident within said parent processor.

Studor discloses where the act of controlling includes initiating at least one of said first and second macro functions using an instruction decoded in the instruction decode stage of the parent processor; where the act of controlling further includes controlling at least one of said macro functions based at least in part on one immediate operand derived from the decoded instruction; or where the act of controlling includes accessing at least one extension register resident within said parent processor (*see generally*, column 3, lines 10-36; column 5, lines 64067 to column 6, lines 1-58).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the extensible processor of Studor with the processor interface

device of Blackmon. The suggestion or motivation for doing so would have been to allow a prior art CPU to be made extensible so that circuitry can be easily added to the extensible processor in order to meet differing customer needs, both in the present and in the future. This significantly reduces the cost for individual customer flexibility (*see* column 2, lines 57-67 and column 3, lines 38-43).

Therefore, it would have been obvious to combine Studor with Blackmon to obtain the invention as specified in claims 1-4, 9, 10, 14, 15, 20-22, 25, 31-34, 44, and 45.

15. Claims 1-3, 9, 10, 31, 32, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,125,429 to Goodwin in view of Studor.

With regard to claims 1, 9, 10, 25, 30, 31, and 44, Goodwin discloses a processor interface device (Fig. 1, item 10) including at least one memory port (not shown), the memory ports adapted to transfer data and signals to and from a storage device (Fig. 1, items 30, 32, 34, and 36), at least one function port (not shown), the function ports adapted to transfer data and signals to and from a macro function (Fig. 1, items 20, 22, 24, and 26), a data transfer fabric (Fig. 1, item 12) adapted to transfer data and signals between the memory ports and the function ports, and an arbitration unit (Fig. 1, 14) adapted to arbitrate access to various portions of the storage device by the macro functions.

With regard to claims 2, 3, 32, and 45, Goodwin discloses a processor interface device, where the data transfer fabric is a crossbar switch fabric (Fig. 1, item 12), and

where the processor interface device further includes a macro function in data communication with the function ports, the macro function being controlled at least in part by a processor instruction associated with the macro function, where the macro function may access the at least one memory port.

Goodwin does not expressly disclose where the processor interface is used in an extensible processor. Studor discloses an extensible processor (*see generally*, Fig. 2).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the extensible processor of Studor with the processor interface device of Goodwin. The suggestion or motivation for doing so would have been to allow a prior art CPU to be made extensible so that circuitry can be easily added to the extensible processor in order to meet differing customer needs, both in the present and in the future. This significantly reduces the cost for individual customer flexibility (*see* column 2, lines 57-67 and column 3, lines 38-43).

Therefore, it would have been obvious to combine Studor with Goodwin to obtain the invention as specified in claims 1-3, 9, 10, 31, 32, 44, and 45.

16. Claims 5-8, 11-13, 16, 17, 35-37, 40-43, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of Studor, as applied to claims 1 and 9, above, and further in view of Gove.

As described above, Blackmon in view of Studor teaches all the features of claims 1-4, 9, 10, 14, 15, 25, 31-34, 44, and 45, and teaches the features of claims 37

and 40-43 that are identical to those features found in claims 1-4, 9, 10, 14, 15, 25, 31-34, 44, and 45.

With regard 5, 7, 8, 35, and 36, Blackmon in view of Studor does not expressly disclose a processor interface device, where the at least one macro functions is controlled by at least one processor instruction associated with an instruction set of a parent processor, where data is processed in a pipeline fashion.

Gove discloses a processor interface device, where the at least one macro functions is controlled by at least one processor instruction associated with an instruction set of a parent processor, where data is processed in pipeline fashion (Fig. 1, item 12).

With regard to claims 6, 16, 40, 41, and 46, Blackmon in view of Studor does not expressly disclose the processor interface device where the parent processor is a RISC processor and where the second data processor is a digital signal processor.

Gove discloses a processor interface device where the parent processor is a RISC processor and the second data processor is a digital signal processor (column 14, lines 46-56).

With regard to claims 11-13, 17, 21, 22, 42, and 43, Blackmon in view of Studor does not expressly disclose the device where at least one function controller has a plurality of registers. Gove discloses the claimed features as described in column 12, lines 20-50).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the parent processor of Gove with the processing interface

device used in an extensible processor of Blackmon in view of Studor. The suggestion or motivation for doing so would have been so that the main processor could assure an orderly flow of data (column 7, lines 35-38).

Therefore, it would have been obvious to combine Gove with Blackmon in view of Studor to obtain the invention as specified in claims 5-8, 11-13, 16, 17, 35-37, 40-43, and 46.

17. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackmon in view of Studor, further in view of Gove, as applied to claim 37 above, and further in view of U.S. Patent No. 6,581,191 to Schubert, et al. ("Schubert").

With regard to claims 38 and 39, and as discussed above, Blackmon in view of Studor, further in view of Gove, discloses all the features of claim 37.

Blackmon in view of Studor, further in view of Gove does not expressly disclose a software wrapper associated with the DSP to translate at least some signals exchanged between said DSP core and the standardized interface; or where the software wrapper includes an HDL wrapper, the HDL wrapper being configured, at least in part at the time.

Schubert discloses a software wrapper and where the software wrapper is an HDL wrapper (column 9, lines 15-21 and column 28, lines 39-43).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the software wrapper of Schubert with the processor interface used in an extensible processor of Blackmon in view of Studor, further in view of Gove.

The suggestion or motivation for doing so would have been to support regression testing of the instrumented design using functional simulation (column 28, lines 39-43).

Therefore, it would have been obvious to combine Schuber with Blackmon in view of Studor, further in view of Gove to obtain the invention as specified in claims 38 and 39.

Response to Arguments

18. Applicant's arguments, see pages 13-16, filed May 26, 2004, with respect to the rejections of claims 1-4, 9-10, 14, 15, 18, 19, and 25 under 35 U.S.C. 102(e) and claims 5-8, 11-13, 16, 17, and 20-22 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection is made in view of U.S. Patent No. 5,848,289 to Studor, et al. and U.S. Patent No. 6,581,191 to Schubert, et al.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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